

# **A Low Power Dynamic TCAM Using Master Slave Match Line Architecture in HSPICE**

A. Tharun kumar <sup>1</sup>, Dr. K. Padma Priya <sup>2</sup>

P.G. Student(VLSI), Department of Electronics & Communication Engineering, University College of Engineering,  
Kakinada, Kakinada, Andhra Pradesh, India<sup>1</sup>

Professor, Department of Electronics & Communication Engineering, University College of Engineering, Kakinada,  
Kakinada, Andhra Pradesh, India<sup>2</sup>

**ABSTRACT:** The focus of this paper is that the coming up with of TCAM using Master Slave Match Line style. Typically CAM may be a memory that has parallel comparison feature used in quick hunt applications. Attributable to this feature massive power consumption takes place in CAM. Thus a brand new design known as MSML style is projected which mixes the master – slave design and charge refill minimization technique to cut back the power consumption. In standard CAM style only one ML is employed, here Master ML and Slave MLs are accustomed to perform search operation. By sharing the voltage between MML and Mismatches SMLs, this style will minimize the MML charge refill swing specified power is reduced effectively. Within the projected style TCAM cell with reduced number of transistors and capability of hold on don't cares in the stored data. The enforced style has best in power reduction and energy consumption in comparison to the existed CAM styles.

**KEYWORDS:** CAM, TCAM, Match Line, MSML, SML, Charge refill minimization.

## **I. INTRODUCTION**

Content Addressable Memory[1] may be a variety of memory that's self-addressed by the content instead of memory location. This memory is of two types: Binary CAM and Ternary CAM. Binary CAM is that the simplest variety of CAM that uses information search words consisting of solely 1's and 0's. Ternary CAM permits a third matching state of 'X' or don't care of one or a lot of bits within the hold on information word, therefore adding flexibility to go looking. Thanks to it's parallel nature, CAM is way quicker than RAM for looking out. ML's are the foremost power consumers in CAM[2]. The ML may be a long wire with giant capacitance, and each search can cause a large quantity of switching activity. Therefore ancient NOR kind CAM ML design provides best performance however it prices an outsized ML power consumption. So, a replacement MSML design will aim at to scale back power by combining Master ML and Slave ML's with charge sharing in between them. This may reduce the specified charge refill swing within the MML in case of Mismatch conditions.

In this paper the projected style were applied to 32-bit, 64-bit and 128-bit CAM word every having MS1, MS2, MS4, MS8 and MS16 five configurations respectively, using TSMC 35-nm technology process with 4 V provide voltage. Besides MSML BCAM and MSML-HP BCAM, standard CAM were designed. All the experimental results are obtained from HSPICE simulation. The experimental results show that this style is appropriate for CAM array with massive word size. All the results are compared between standard CAM MSML BCAM, MSML-HP BCAM and MSML TCAM. The TCAM style using this method is that the best for low power and low energy consumption with MS16 configuration.

This paper is organized as follows, section 2 represents Literature survey of CAM cells. Section 3 describes Existing ML architectures. Section 4 introduces proposed MSML method with complete operation in detail. Section 5 represents Experimental comparison results. Section 6 represents Conclusion.

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## II. LITERATURE SURVEY OF CAM CELLS

### A. EXISTED CAM CELLS:

#### 1. XOR BCAM Cell:

The CAM consists of principally two components :1) one for storing data, referred to as store unit; and 2) the other for comparing data , referred to as compare unit which is shown in Fig.1. The store unit is typically implemented as 6T SRAM cell that contains cross coupled inverter pair. The compare unit is pass transistor logic for comparing the stored with search data. Besides the store and compare unit, a pull down transistor M, that is gate controlled by the comparison result, is necessary to connect/disconnect the ML to/from the ground.

#### 2. XNOR BCAM Cell:

In Fig.1 the XOR BCAM cell could be a straight forward nmos PTL circuit, there's Vt drop at compare output. Therefore the transistor M may be turned OFF utterly, however cannot be absolutely turned ON. This causes the charge sharing speed between SML and MML is reduced. To eliminate this drawback an extra changed BCAM cell is shown in Fig.2. This BCAM cell uses the XNOR compare unit with the addition of Inverter to drive that result. This inverter makes the transistor M may be absolutely turned ON and therefore charge sharing speed will increase between the MML and SML, however with penalty of tiny increase of power.

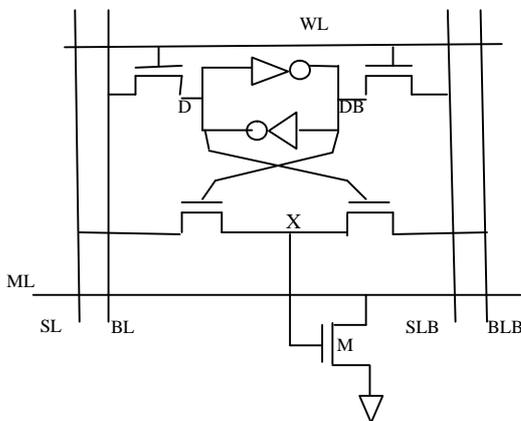


Fig.1. XOR BCAM cell

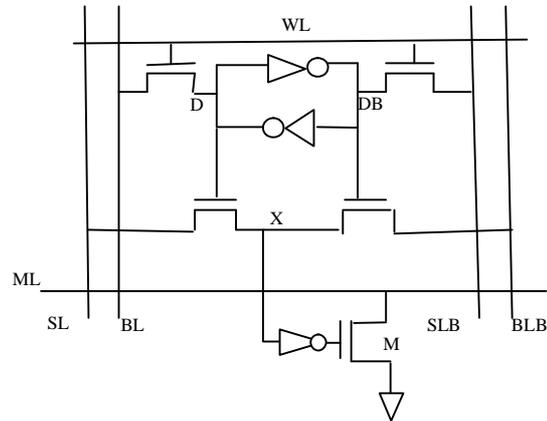


Fig.2. XNOR BCAM cell

### Write Operation :

Write operation starts once Write Line is high and also the corresponding values has given to bit lines. At this time no search information and no precharge to ML. The table.1 shows the stored operation of BCAM cell. During Write operation, whenever both the bit lines are same this BCAM isn't allowed to store the bit and otherwise it stores the worth that is same as bit line value.

### Search operation:

During this operation WL goes to Low, precharge ML to high and search information has given to look lines. Whenever mismatch happens the comparator output is high and it causes the M junction transistor ON to connect ML to the ground otherwise the output is zero and it disconnects ML from the ground.

### B. Proposed CAM cell:

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The Fig.3 Shows the Dynamic TCAM cell style[2] in which the store unit is totally different from the BCAM. The store unit has two capacitors rather than SRAM unit for storing data. The subsequent table.2 shows the stored operation of DTCAM cell.

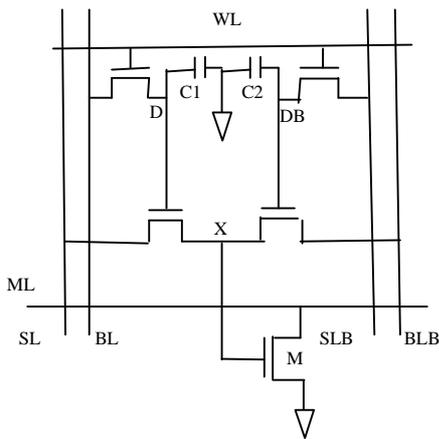


Fig.3 Dynamic TCAM cell

BL	BLB	D
0	0	Not allowed
0	1	0
1	0	1
1	1	Not allowed

Table.1 Stored bits of BCAM

BL	BLB	D
0	0	X
0	1	0
1	0	1
1	1	Not allowed

Table.2 Stored bits of DTCAM

The table.2 clearly tells that it stores don't care bit in stored data whenever both the bit lines are 0. The write and search operation is same as that of BCAM cell except that storing X worth in write operation. Thus it is adding flexibility to the search operation and uses capacitor model[6] to store bit at respective nodes. TCAM is an important component for many applications especially network. For rapidly growing size of routing tables brings with it the challenge to design higher search speeds and lower power consumption.

### III. EXISTED MATCH LINE ARCHITECTURES

#### 1. Conventional NOR ML Architecture:

In this kind of existing style [2] all the pull down transistors of every CAM cell unit are arranged in NOR sort that is shown in the Fig.4. For a CAM word, if one or lot of cells are mismatched, the ML would be discharged to zero. Only when all cells are matched, the ML will retain logic high as within the precharge phase. As a result of the pull down path is extremely short, just in case of mismatch the ML is discharged to 0 quickly. Thus it is power inefficient in search operation and results in the MSML style.

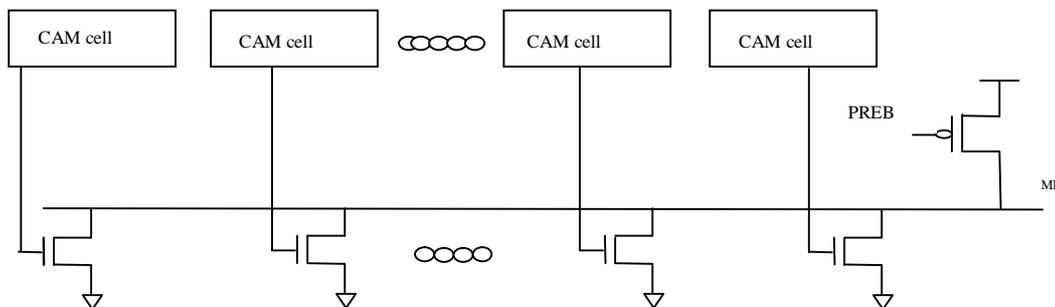


Fig.4 Conventional NOR type ML

#### 2. Segmented ML Architecture:

Due to typical NOR ML design power consumption is incredibly high in order that this SMA ML design[3] was projected. In this design the overall ML was divided into four segments which is shown in fig.5. These segments consists of two precharged segments and two charge shared segments each respectively. The operation starts by

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precharging the pre-charged segments with SP signal and so with the assistance of CS charge was shared between segments. Because only the precharged part need to be charged, the ML power consumption can be profitably decreased.

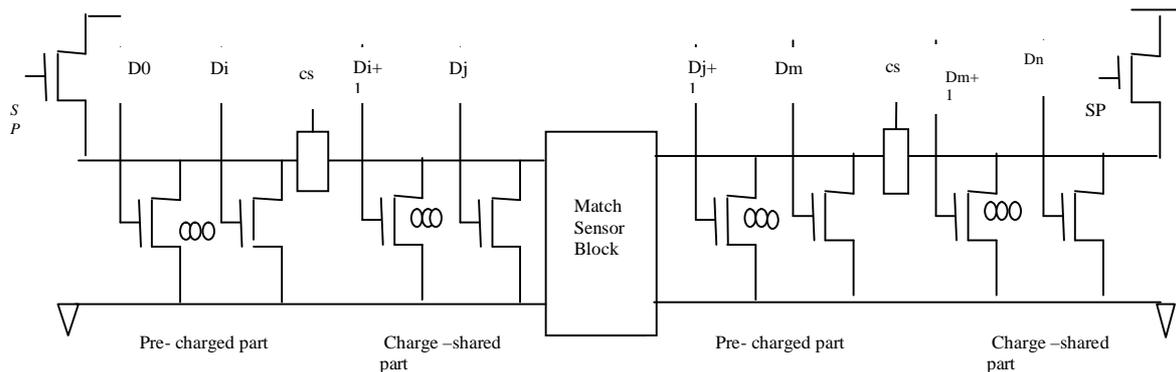


Fig.5 SMA ML Architecture

## IV. MSML DESIGN

The main theme of this style is to mix the master slave design with the charge refill minimization[5] technique to reduce the ML switching power. The options of the MSML style are as follows:

- 1) The MSML style uses one Master ML and several other Slave MLs to perform the search operation.
- 2) Instead of discharging the whole MML to 0, solely the Mismatched SMLs would draw the charge from MML, and then be discharged.
- 3) The refill charge to MML is much less than the entire ML charge refill within the NOR kind ML design, the match line power may be reduced effectively.
- 4) Power saving is guaranteed as a result of it saves power even in worst case conditions because it is independent on the search data and mismatch situation.

The Fig.6 Shows a MSML style example MS2, that consists of one MML and two SMLs. Besides the MML and SML, a further Final ML is employed to point the match result. In each CAM search operation there are two phases: 1) Precharge Phase 2) Match Evaluation Phase.

### 1. Precharge Phase:

In this phase, the control signal PRE is high. Therefore MML and FML are precharged to high, and all SMLs shown in Fig.5 are discharged to zero. This can be as a result of the search data is not available in this phase, and therefore the charge sharing paths between MML and SML, i.e., S1 and S2 are disconnected in this phase.

### 2. Match Evaluation Phase:

In this phase the control signal PRE is pulled to 0 and search data got to be loaded on the search lines to begin the matching process. The cam word should divide into two SML segments i.e., SML1 and SML2 as shown in Fig.6. Depending on the match results of every SML there are four attainable cases in this phase.

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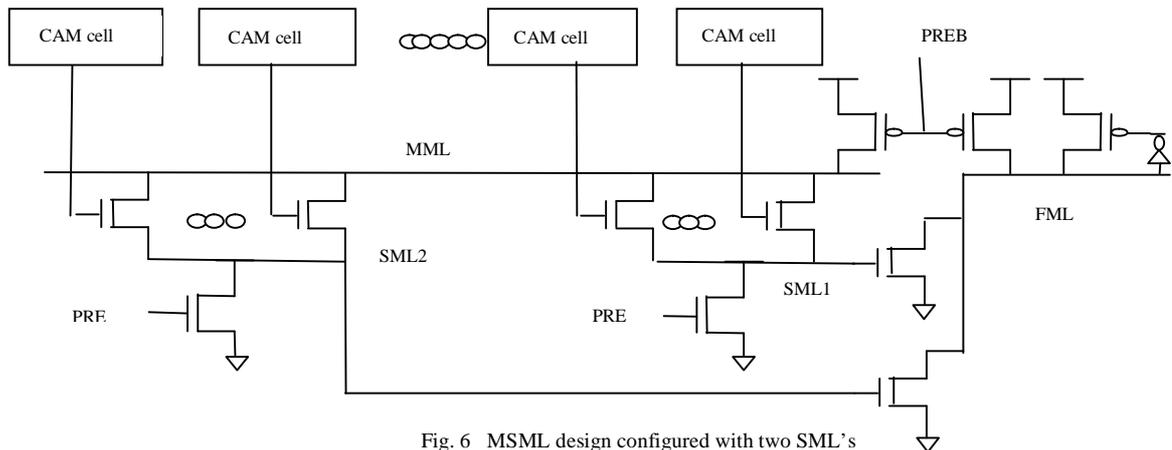


Fig. 6 MSML design configured with two SML's

### Case I (Both SML1 and SML2 are match)

This is the sole match case during which both the charge sharing paths S1 and S2 do not conduct. The FML and MML are same as in precharge phase i.e., high and all SMLs are 0.

### Case II (Either SML1 or SML2 is Mismatch)

In this case either SML1 or SML2 is mismatch and alternative one is match. If SML1 is mismatch the charge sharing path S1 is ON to share the charge between MML and SML1. This ends up in increase of SML1 voltage where as the MML voltage goes down. After the complete charge sharing both the MML and SML1 finally saturated at the equivalent voltage i.e., final balance voltage. According to the voltage sharing equation[4], the final balance voltage VB is given as:

$$VB = (CMML/CMML+CSML1)*VMML$$

$$VB = (2/3) VMML$$

Where CMML and CSML1 are the capacitances of MML and SML1 respectively, and VMML is that the MML initial voltage. Because the MML capacitance is roughly double the SML1 capacitance, the result can be simplified as above.

### Case III (Both SML1 and SML2 are mismatch):

In this case both SML1 and SML2 segments are mismatch as a result of the charge sharing path S1 and S2 are conducted, the MML charge are going to be distributed to the SML1 and SML. The final balance voltage VB is given as:

$$VB = (CMML/CMML+CSML1+CSML2)*VMML$$

$$VB = (1/2) *VMML$$

The table.3 lists the final balance voltage of 128 bit MSML style with different configurations under room temperature and supply voltage VDD=4v.

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MS Configurations	Final Balance Voltage
MS1	2.850
MS2	2.165
MS4	1.383
MS8	1.045
MS16	0.696

Table.3. Final balance voltage for 128 bit MSML design

## V. EXPERIMENTAL RESULTS

### A. MSML DESIGN WAVEFORM:

The Fig.7 Shows the waveform of MSML style search output waveforms. From the waveforms it's clearly shows that the MML and SML voltage is sharing between them when the mismatch occurs everytime. The FML reduces to zero when the mismatch case occurs otherwise it remains as high as precharge phase. Due to this the charge refill swing for MML reduced compare to the NOR ML style[2]. So the power consumption is effectively reduced compared to previous design.

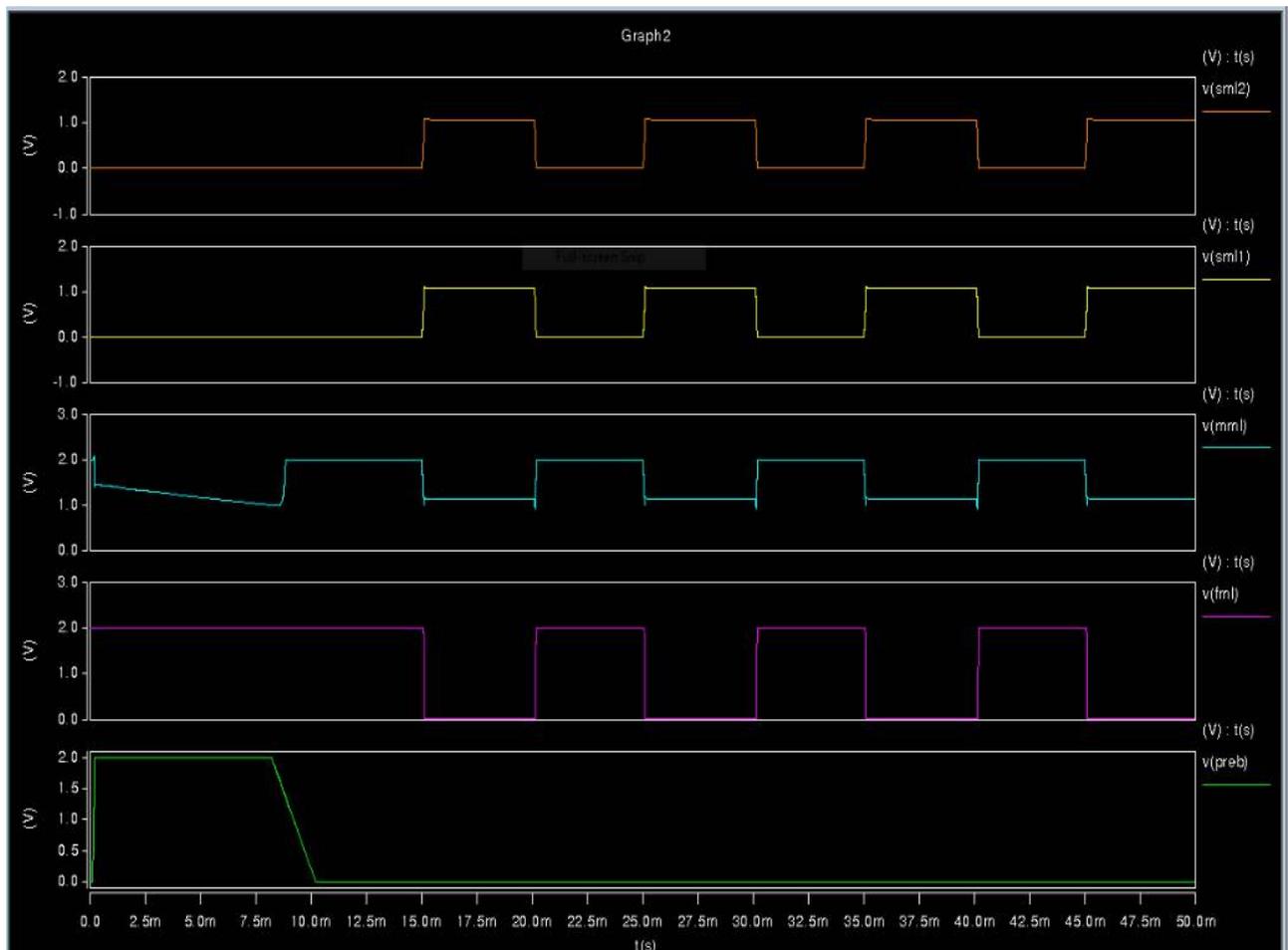


Fig.7 MSML TCAM/BCAM Design search operation Waveform.

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### B. POWER DISSIPATION:

The Table.4 represents the power dissipation of 128 bit word CAM of varied styles. It clearly depends on the ML capacitance i.e., word size, and varies with Mismatched SML within the MSML style. From the power results NOR type ML costs immense dissipation compare to other designs. MSML-HP BCAM prices power penalty compared to MSML BCAM and MSML TCAM due to insertion of inverter. Clearly large SML number is beneficial to power reduction. The MSML TCAM which even result in more than 50% power improvement compared to other MSML BCAM and MSML HP\_BCAM depending on the master slave configuration.

CAM WORD TYPE	MS1	MS2	MS4	MS8	MS16
MSML TCAM	1.447e-07	5.990e-07	5.925e-07	6.070e-07	9.060e-06
MSML HP_BCAM	3.637e-06	7.071e-06	1.511e-05	1.510e-05	2.615e-04
MSML BCAM	1.817e-06	1.878e-06	1.399e-05	1.331e-05	2.721e-05
CONVENTIONAL CAM	5.284e-04				
SMA CAM	1.186e-04				

Table.4. Comparison of Power for all 128 Bit CAM Designs

### C. PERFORMANCE:

The following Table.5 Shows the worst CAM performance for 128 bit word for varied CAM styles. From the waveforms with the extra inverter the MSML-HP BCAM will improve the MSML performance effectively compared to other CAM designs. As a result of the charge sharing is fast between the large MML and small SML, the MSML performance increases with SML segment number. In the 128 bit word size case the MSML TCAM MS8 performance is the best performance across all designs. The MSML TCAM has 54 % and 85% improvement in performance aspect compared to MSML BCAM and MSML HP\_BCAM in the MS16 configuration respectively.

CAM WORD TYPE	MS1	MS2	MS4	MS8	MS16
MSML TCAM	1.93e-06	1.85e-06	1.93e-06	1.62e-6	1.492e-06
MSML HP_BCAM	4.114e-06	3.650e-06	3.234e-06	3.148E-06	3.051e-06
MSML BCAM	14.98e-06	12.93e-06	11.91e-06	11.30e-06	10.490e-06
CONVENTIONAL CAM	15.49e-06				
SMA CAM	4.649e-05				

Table.5. Comparison of Performance for all 128 Bit CAM Designs

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**D. ENERGY CONSUMPTION:**

The Following Table.6 Shows the energy consumption of 128 bit word Varied CAM styles. All together cases compared with original MSML BCAM and MSML-HP BCAM design MSML TCAM has better energy efficiency. Normally we are able to improve the energy efficiency by increasing the SML number. However due to MS design this rule is not valid in little word size case. In 128 bit word MSML TCAM the ML energy efficiency is best for MS16 configuration with 52.4% and 89.5% better improvement than MSML BCAM and MSML HP\_BCAM respectively.

CAM WORD TYPE	MS1	MS2	MS4	MS8	MS16
MSML TCAM	7.091e-07	7.091e-07	3.903e-07	3.504e-07	3.439e-07
MSML HP_CAM	1.782e-07	3.465e-07	7.404e-07	7.397e-07	7.281e-07
MSML BCAM	8.903e-06	3.571e-06	3.855e-06	3.592e-06	3.293e-06
CONVENTIONAL CAM	2.589e-05				
SMA CAM	5.810e-06				

Table.6. Comparison of Energy for all 128 Bit CAM Designs

**E. ENERGY DELAY PRODUCT:**

The following Table.7 Shows the EDP of 128 bit word of varied CAM styles. Compared to the MSML BCAM and MSML-HP BCAM, the design MSML TCAM has improved EDP. For the MS16 configuration MSML TCAM design has better EDP with 84.5 % improvement than MSML HP\_BCAM.

CAM WORD TYPE	MS1	MS2	MS4	MS8	MS16
MSML TCAM	1.059e-08	4.358e-12	4.334e-12	2.244e-12	6.622e-12
MSML HP_BCAM	7.332e-08	5.718e-09	6.837e-09	6.999e-09	4.166e-11
MSML BCAM	3.560e-08	5.332e-08	5.339e-08	5.356e-08	4.908e-08
CONVENTIONAL CAM	3.852e-07				
SMA CAM	2.701e-10				

Table.7. Comparison of EDP for all 128 Bit CAM Designs

## VI. CONCLUSION AND FUTURE WORK

In this paper a low power ML style referred to as MSML style was introduced, within which we have a tendency to mix master- slave design with charge refill step down technique takes place to reduce power. The HSPICE results shows that the MSML TCAM is suitable for giant size word rather than little word size CAM words. Returning to performance the MSML-HP CAM is nice compared to other MSML styles. This design saves power even within the worst case conditions and plenty of power is guaranteed. Future for smaller CAM words better architecture than this

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design may be introduced with superior performance in all aspects.

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